Brief report of the organized event
(Financial Assistance to Seminar / Symposia)

Date: 30.07.2022

SERB Sanction / File No: SERB File Number: SSY/2022/000201

1. Name of Academic Institution / University / ~~Society~~ etc. under whose auspices the ~~Seminar / Conference~~ / Workshop / ~~Symposium etc.~~ was organized:
Koneru Lakshmaiah Education Foundation (Deemed to be University), Vaddeswaram, Guntur, A.P

2. Title of the Seminar / Conference / Workshop / Symposium etc.:

"Recent advancements in VLSI Chip Devices/Circuits and its Applications"

3. Duration / Period of the organized event: 5 Days (20/06/2022 to 24/06/2022)

4. Grant Sanctioned: Rs.75,000/-

5. Summary of the event (Max. 1000 Words):

National Workshop on "**Recent advancements in VLSI Chip Devices/Circuits and its Applications**" Organized by Microelectronics s Research Group, Department of Electronics & Communication Engineering, KL University, Green Fields, A.P, India

On behalf of the Microelectronics Research Group, we are happy to announce that we have conducted 5-Days National Workshop on "**Recent advancements in VLSI Chip Devices/Circuits and its Applications**" on **20th-24th, June, 2022** successfully.

We have invited resource persons from premier Institutions like IIT's NITS, Deemed University and other Engineering Institutions. We have invited all higher academic officials Hon'ble Vice Chancellor, Hon'ble Pro-VC, Respected Principal, Deans, HoD's, Faculty members, participants from other Institutions, research scholars, and Press & Media for Inauguration function on 25th, July, 2022@9.30. This workshop is supported by Science Engineering Research Board (SERB), **Department of Science and Technology (DST), New Delhi** .

Our Hon'ble Chancellor, Vice Chancellor, Principal, Head of the Dept, other dept Deans, Heads, Professors attended the inauguration of the Workshop. Our Hon'ble Vice Chancellor Dr.GPS Varma attended inauguration session and shared his valuable speech on "**importance of miniaturization concepts in the present era**". Our Hon'ble Pro-VC Dr.N Venkatram shared his valuable speech on "**latest developments on IC**" and our institution collaborated with IIT Hyderabad, IIT Bombay and IISc Bangalore. He says that this kind of multidisciplary research works gives lots important and yields to the University and also to the Nation. Our Principal, Dr.Rama Krishna Rao says, microelectronics is leading our electronics industry and this type of research forums really gives good knowledge to the research Scholars and students.

Day-1

Morning Session: We have called **Dr.Gopal Rawat** from **NIT Hamirpur** for first day morning session and he gave a talk "**Future roadmap Electronics Industry**" and afternoon session we have **Dr.K.Srinivasa Rao**, given talk on "Recent development of semiconductor nanoscale devices" and we have **Dr.Balawindar Rai, NITTTR**, Chandigarh, given talk on "**Multi Gate TFET Devices**".

Day-2

Dr.KaviChanran from NIT Silchar has given a talk on "**Analysis of Source Engineered Asymmetric Tunnel FETs".** He has given clear understanding about TFET devices and its issues and possible solutions. **Dr.A.Narendra Babu,** LBRCE, JNTU Kakinada has given a talk on **"Learning algorithms for VLSI design automation". Dr.Santosh Kumar Viswakarma, IIT Indore has given talk " Hardware Accelerator for VLSI Circuits".**

Day-3

Dr.Sangeetha singh from NIT Patna given a talk on "**Charge-Plasma FET and State of the Art Advanced Semiconductor Devices ".** She has focus on TFET devices, particularly Charge Plasma FET for Bio-Sensing applications. **Dr.Keerthi, BVRIT, JNTU Hyderabad** has given a talk and hands on session " TCAD tool for device Simulation" **Dr.Ekta Goel from NIT Warangal given talk on " Semiconductor devices and Engineering solutions towards Industry Needs.**

Day-4

Dr.Asish Raman from NIT Jalamdar has given a talk on "**Charge-Plasma FET and State of the Art Advanced Semiconductor Devices "** . He has talk about present state of all kind of VLSI Chip Devices and its applications. **Dr.Ashok Kumar, SVEC, JNTU Kakinada** has given hands on session "TCAD-Circuit simulation by Synopsys". **Dr.Suman Latha Tripathy**, from Lovely Professional University has give talk and hands on session. " TCAD Tools device Simulation"

Day-5

Morning Session, we have **Dr.Girish Wadwa, NIT Jalamdar**, given a talk on "TFET Devices towards for Biosensing Applications". He discussed very important points of TFET Devices, variety of biosensors, Sensing applications from TFET etc. Dr.K.Girija Sravani, "**Aging challenges for AI applications "**and last Session is talk given by **Dr.Biswajit Jene, VIT University** Chennai on "TCAD Tool for TFET Device Simulation-Hands on Training".

The total number of participants for this workshop is 100 members; they have attended from around the state, few members from out of state too. The organizing committee has done excellent job, without any discrepancy and disturbance in any aspects.. Finally, as Convener Dr.K.Girija Sravani and Co-Conveners Dr.B Balaji & Dr.K.Srinivasa Rao says vote of thanks to resources, & participants for making the workshop a grand success.

(Convener Signature)

Participation Information:

Sl.No	Participation in the event	No's
I	**Key-not speakers**	10
II	**Senior Scientist**	5
III	**Young Scientist**	25
IV	**Postgraduate Students**	35
V	**Undergraduate Students**	10
VI	**Industry persons**	
VII	**Other category (Please specify each category)--Faculty Members**	30

Photographs Section: Please paste high resolution photographs in given spaces below or may be submitted directly on online / email in JPEG format.

1. **Inaugural Session**

Electronics & Communication Engineering

SERB Sponsored National Workshop
On
Recent Advancements in VLSI Chip Devices/Circuits and its Applications
Organized
by
Microelectronics Research Group (MERG)
Department of Electronics & Communication Engineering
(DST - FIST Sponsored Department)
Koneru Lakshmaiah Education Foundation

Vote of Thanks

Electronics & Communication Engineering

SERB Sponsored Faculty Development Program
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COORDINATOR
Dr. K. Girija Sravani, Assoc. Professor, Dept of ECE, KL Deemed to be University

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SERB Sponsored Faculty Development Program
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Dr. G. Pardha Saradhi Varma, Vice-Chancellor, KL Deemed to be University

Dr. N. Venkatram, Pro-Vice Chancellor, KL Deemed to be University

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Dr. Rama Krishna Rao TK Principal, KL Deemed to be University

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Dr. M. Suman, HOD, Department of ECE, KL Deemed to be University

2. **General Photograph**

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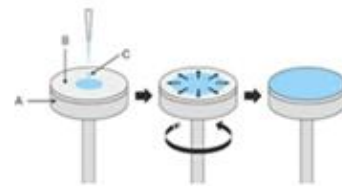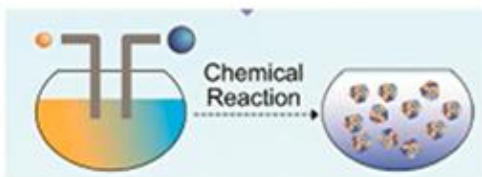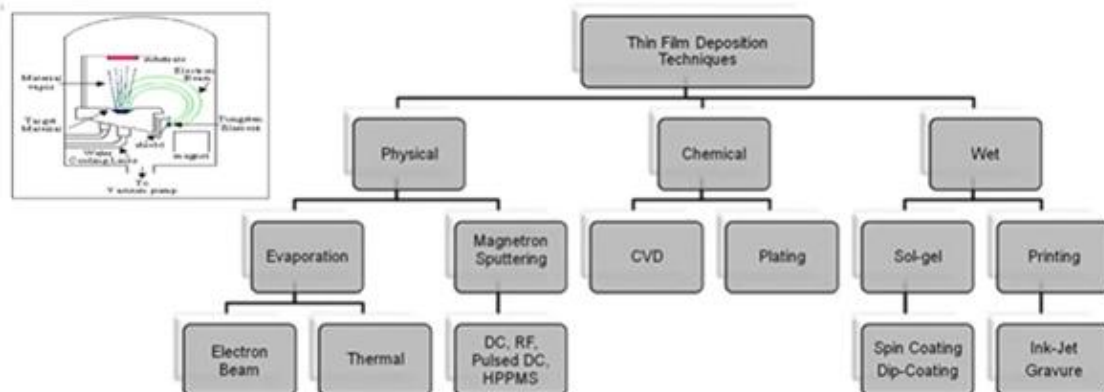Koneru Lakshmaiah Education Foundation

Time:
10.00 AM to 11.30 AM

Topic:
**Future Roadmap of Electronics
Industry**

**Dr. Gopal Rawat,
NIT Hamirpur**

BUSINESS FOOTPRINT OF ELECTRONICS INDUSTRY

COMPETITIVE CLUSTER

| SATELLITE TECHNOLOGY | CIRCUIT BOARD AND CONTRACT MANUFACTURING | TELE-COMMUNICATIONS (NOT CELL PHONES) | MEDICAL TECHNOLOGY | CONSUMER ELECTRONICS | APPLIANCES |

Key Segments of Electronics Industry

- Semiconductor supply and manufacturing services
- Industrial Equipment
- Networking and Communication Equipment
- Computer and Office Products
- Medical Devices
- Consumer electronics and home appliances

What are Electronics Industry Value Chain ?

1. **Product & Service Development**
2. **Procurement, Supply, & Manufacturing**

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Time: 2p.M to 3.30P.M

Topic:Multi-Gate Devices for VLSI Design

Dr.Balawindar Raj, NITTTR Lucknow

3. **General Photograph**

Nanoscale Device: Problems

The problem is not only at process level but also at device design level. The SCE (short channel effects) which is basically roll-off of threshold voltage due to interference of drain field at source side.

SCE: Not only barrier lowering problem but also several other issues have come up such as:

- Punch through
- Hot electron effect
- source/drain series resistance,
- Leakage currents.

NITTR Chandigarh

Dept. of ECE

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Dr. K. Srinivasa Rao, KL Deemed to be University.Head-Microelectronics Research Group

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Time:
2.00 PM to 3.30 PM

Topic:

Hands-on Session: nm CMOS PDK, EDA Tools for Circuit Design

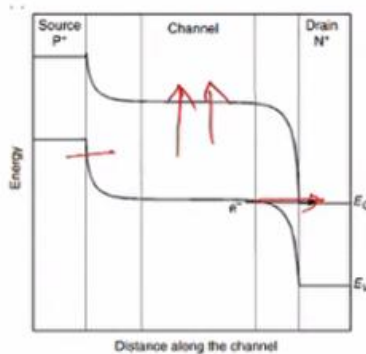**Dr. Ekta Goel, NIT Warangal**

Ambipolar behaviour:

- TFET devices have a tendency of showing ambipolar behaviour i.e it can generate current at negative Vgs.
- An introduction of negative Vgs makes the bands of the channel move upward thus making it aligned with the drain side CB.
- Charge carriers move from VB of channel to CB of drain.

Figure 8 Band Diagram of TFET in ambipolar state when Gate voltage is negative

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Time: 11A..M to 12.30P.M

Topic: TCAD-Circuit simulation by Synopsys

Dr.P.Ashok Kumar, SVEC, JNTU Kakinada

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Time:
2.00 PM to 3.30 PM

Topic:

Hardware Accelerator

Dr.Santhosh Kumar,

IIT Indore

Cloud AI Computing

In the cloud, GPU, especially NVIDIAs' series GPU chip, have been widely used to do classification and to train deep neural networks. The GPU with thousands of computational cores can achieve 10-100x application throughput compared to CPUs alone, GPU accelerators are still main stream for machine learning for many of the largest web and social media companies. **NVIDIAs' Tesla V100** is specially designed for Deep learning which incorporates Tensor Cores with GPU cores, could provide 120 TFLOPS (120 trillion floating point instructions per second) processing power. Moreover, NVIDIAs' GPU also has an excellent software development environment, which is one of the most widely used platforms in the field of AI training.

4. **General Photograph**

Introduction: Devices for CMOS Extension

Fabrication Issues

As per IRDS

- Carbon Nanotube FETs ✓
- 2D Material Channel FETs ✓
- Nanowire FETs ✓
- Tunnel FETs
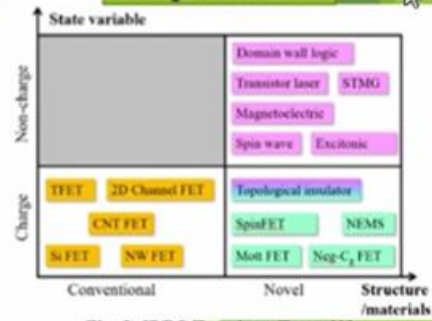
Other Solutions:
- Integrated high-k dielectrics with EOT <0.5nm and low leakage.
- Integrated contact structures that have ultralow contact resistivity.
- Achieving high hole mobility in III-V materials in FET structures.

Fig. 3. IRDS Transistor Types [3]

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Time: 2p.M to 3.30P.M

Topic: Aging challenges for AI applications

Dr.K.Girija Sravani,
Associate Professor, KLU

VELLORE INSTITUTE OF TECHNOLOGY, CHENNAI

Dr. Biswajit Jena
Assistant Professor (Sr. G2)
School of Electronics Engineering (SENSE)

Micro and Nano Devices Group

TCAD TOOLS FOR DEVICE SIMULATION

Area of Research: Nano Scale Device Modeling and Simulation,

Technology Computer Aided Design (TCAD)

- Technology Computer Aided Design (TCAD) is the integration of computational methods and software tools for the design and study of semiconductor devices and their production processes. Usually a single device, or small group of devices is analyzed using TCAD tools.

- Here, the device, or, in the early stages of production, a sub-region of a wafer, is modelled by a binary representation of its properties. e.g., its geometry, its material, dopant concentrations, and temperature distribution in two or three dimensions.

- Process simulators are a set of numerical simulation tools that show how the real device is made. They show how the steps in the process flow.

- Lastly, the semiconductor transport equations are solved in the newly made transistor by a device simulator, which figures out how the transistor will behave electrically.

- **Using TCAD, predictions will be made about technological issues before the actual devices have to be made. This cuts down on the cost and time of developing a process.**

(Convener Signature)